CLAIMS

What is claimed is:

1. A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction of change in voltage of said input signal; and

introducing a current to said parasitic capacitance to compensate for current of said input signal charging said parasitic capacitance responsive to detection of a positive edge of said input signal.

2. The method of claim 1, wherein said signal is applied to an input of an input/output device.

3. A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction of change in voltage of said input signal; and

preventing discharge of said parasitic capacitance responsive to detection of a negative edge of said input signal.

4. A method for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising the steps of:

detecting a change in voltage of said input signal; and

changing an impedance of a parallel termination circuit that is in parallel with said parasitic capacitance to reduce distortion of said input signal.

5. Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising:

a detection circuit for detecting a change in voltage of said input signal coupled to said input; and

a correction circuit coupled to said detection circuit for compensating for current from said input signal that would be diverted to said parasitic capacitance due to a positive edge of said input signal.

6. The apparatus of claim 5, wherein said detection circuit includes a capacitance.

7. The apparatus of claim 5, wherein said circuit is an input/output device.

8. Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising:

a detection circuit for detecting a change in voltage of said input signal coupled to said input; and

a correction circuit coupled to said detection circuit for compensating for preventing current from said parasitic capacitance to be added to said input signal due to a negative edge of said input signal.

9. The apparatus of claim 8, wherein said detection circuit includes a capacitance.

10. The apparatus of claim 8, wherein said circuit is an input/output device.

11. Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising the steps of:

a detecting circuit for detecting a change in voltage of said input signal; and

a correction circuit for changing an impedance of a parallel termination circuit that is in parallel with said parasitic capacitance to reduce distortion of said input signal.

12. A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction in change in voltage of said input signal; and

introducing a current to said parasitic capacitance to compensate for distortion of said input signal due to said parasitic capacitance responsive to detection of a positive edge of said input signal.

13. A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction of change in voltage of said input signal; and

preventing introduction of a current from said parasitic capacitance into said input signal responsive to detection of a negative edge of said input signal.

14. Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising:

a first circuit element for selectively providing current to said parasitic capacitance;

a second circuit element for selectively preventing discharge of said parasitic capacitance into said input; and

a control circuit monitoring said input signal for respectively turning on said first circuit element and turning off said second circuit element when a positive going edge of said input signal is detected and for turning off said first circuit element and turning on said second circuit element when a negative going edge of said input signal is detected.

15. The apparatus of claim 14 wherein said first and second circuit elements have a common terminal coupled to said parasitic capacitance.

16. The apparatus of claim 15 wherein said first and second circuit elements are transistors.

17. The apparatus of claim 16 wherein one of said transistors is a PMOS transistor and another one of said transistors is an NMOS transistor.